S.J.P.N. Trust's

Hirasugar Institute of Technology, Nidasoshi.

Inculcating Values, Promoting Prosperity

Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi

Recognized under 2(f) &12B of UGC Act, 1956

Accredited at 'A' Grade by NAAC & Programmes Accredited by NBA:CSE &ECE

ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT

III SEM COURSE PLAN 2022-23

INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

“To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates.”

DEPARTMENTAL MISSION

“Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool”.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM SPECIFIC OUTCOMES(PSOS)

The graduates will be able to:

PSO1:

An ability to understand the concepts of Basic Electronics and Communication Engineering and to apply them to various areas like Signal Processing, VLSI, Embedded Systems, Communication Systems and Digital & Analog Devices

PSO2:

An ability to solve complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions

PROGRAM OUTCOMES(POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research

methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainble development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and mangement principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sr.No	Name of the faculty	Activities
1	Dr. R. R. Maggavi	GATE / Preplacement Coaching
		CN Lab In charge
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
2	Prof. S. S. Malaj	GATE / Preplacement Coaching
		Adv.Comm. Lab In charge
		Students Mentor
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		NIRF Coordinator
		Conference Coordinator
3	Prof. S. S. Kamate	GATE / Preplacement Coaching
		VLSI Lab In charge
		Students Mentor
		Module Coordinator
		IEEE Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
4	Prof. D. M. Kumbhar	GATE / Preplacement Coaching
		AC Lab In charge
		Students Mentor
		Dept. Association Coordinator
		VII Class Teacher
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Dept. ED Cell Coordinator

Sr.No	Name of the faculty	Activities
5	Prof. S. S. Patil	GATE / Preplacement Coaching
		ARM & ES Lab In charge
		Students Mentor
		III Sem Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Admission Coordinator
		Module Coordinator
6	Prof. D. B. Madihalli	GATE / Preplacement Coaching
		DSD Lab In charge
		Students Mentor
		NBA Coordinator
		News & Publicity Coordinator
		NBA Criteria Coordinator
		Website Coordinator
		VTU LIC Coordinator
7	Prof. P. V. Patil	GATE / Preplacement Coaching
		HDL Lab In charge
		Students Mentor
		NBA Criteria Coordinator
		T&P Cell Coordinator
		Alumni Coordinator
		Project Coordinator
8	Dr. S. S. Ittannavar	GATE / Preplacement Coaching
		DSP Lab In charge
		Students Mentor
		EMS/ IA Coordinator
		News Letter / Technical Magazine
		AICTE Coordinator
9	Prof. B. P. Khot	GATE / Preplacement Coaching
		MC Lab In charge
		Students Mentor
		Dept. Time Table Coordinator & Meeting Coordinator
		V Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator

CONTENTS

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	09	16.76Y
2	Technical supporting staff.	04	22.02Y
3	Helper staff	02	21.50Y

MAJOR LABORATORIES

S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	35.51
2	Analog Electronics (ED &I) Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.50	7	Research/E-Yantra/DSP & C.N.Lab	71	16.49
4	HDL/MC / EMD Lab	71	19.57	8	Power Electronics Lab	--	4.86
Total Investment In The Department						**Rs. 95.31 Lacs**	

FACULTY DETAILS

TEACHING FACULTY

S.N.	Name and Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Dr. R. R. Maggavi	Ph.D	E&C	LMISTE	18Y.05M	9480275583
2	Smt. S. S. Malaj	M.E.	E & TC	LMISTE	25Y.07M	9731795803
3	Smt.S.S.Kamate	M.Tech	Digital Electronics	LMISTE	20Y.00M	9008696825
4	Sri. D.M. Kumbhar	M.Tech	Electronics	LMISTE	18Y.10M	09373609880
5	Sri. Sachin .S. Patil	M.Tech	VLSI & Embedded	LMISTE	18Y.08M	9448102010
6	Sri .D.B. Madihalli	M.Tech	Industrial Electronics	LMISTE	15Y.07M	9902854324
7	Sri.P.V.Patil	M.Tech	VLSI & Embedded	LMISTE	10Y.04M	9731104059
8	Dr.S .S .Ittannavar	Ph.D	DSP	LMISTE	9Y.11M	9964299498
9	Smt. B. P. Khot	M.Tech	Microelectronics & Control Systems	LMISTE	6Y.11M	9964019501

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience (in years)
1.	Sri. P. S. Desai	DEC	22Y-.07M
2.	Sri. V. V. Guruwodeyar	DEC	31Y-02 M
3.	Sri.M.A.Attar	DEC	12Y-09M

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E. in Electronics and Communication Engineering (ECE)

Scheme of Teaching and Examinations 2021

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2021 - 22)

III SEMESTER

Sl. No	Course and Course Code	Course Title	Teaching Department (TD) and Question Paper Setting Board (PSB)	Teaching Hours /Week				Examination				Credits
				Theory Lecture	Tutorial	Practical/ Drawing	Self -Study	Duration in hours	CIE Marks	SEE Marks	Total Marks	
				L	T	P	S					
1	BSC 21MAT31	Mathematics Course (Common to all)	TD- Maths PSB-Maths					03	50	50	100	3
2	IPCC 21EC32	Digital System Design using Verilog	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
3	IPCC 21EC33	Basic Signal Processing	TD: ECE PSB: ECE	3	0	2		03	50	50	100	4
4	PCC 21EC34	Analog Electronic Circuits	TD: ECE PSB: ECE	3	0	0	1	03	50	50	100	3
5	PCC 21ECL35	Analog and Digital Electronics Lab	TD: ECE PSB: ECE	0	0	2		03	50	50	100	1
6	UHV 21UH36	Social Connect and Responsibility	Any Department	0	0	1		01	50	50	100	1
7	HSMC 21KSK37/47	Samskrutika Kannada	TD and PSB HSMC	1	0	0		01	50	50	100	1
	HSMC 21KBK37/47	Balake Kannada										
	OR											
	HSMC 21CIP37/47	Constitution of India and Professional Ethics										
8	AEC 21EC38X	Ability Enhancement Course - III	TD: Concerned department PSB: Concerned Board	If offered as Theory Course				01	50	50	100	1
				1	0	0						
				If offered as lab. course				02				
				0	0	2						
								Total	400	400	800	18

9	Scheduled activities for III to VIII semesters	NMDC 21NS83	National Service Scheme (NSS)	NSS	All students have to register for any one of the course namely National Service Scheme, Physical Education (PE)(Sports and Athletics) and Yoga with the concerned coordinator of the course during the first week of III semester. The activities shall be carried out between III semester to VIII semester (for 5 semesters). SEE in the above courses shall be conducted during VIII semester examinations and the accumulated CIE marks shall be added to the SEE marks. Successful completion of the registered course is mandatory for the award of the degree. The events shall be appropriately scheduled by the colleges and the same shall be reflected in the calendar prepared for the NSS, PE and Yoga activities.
		NMDC 21PE83	Physical Education (PE)(Sports and Athletics)	PE	
		NMDC 21YO83	Yoga	Yoga	

Course prescribed to lateral entry Diploma holders admitted to III semester B.E./B.Tech programs

1	NCMC 21MATDIP31	Additional Mathematics - I	Maths	02	02	--	--	---	100	---	100	0

Note: **BSC:** Basic Science Course, **IPCC:** Integrated Professional Core Course, **PCC:** Professional Core Course, **INT** –Internship, **HSMC:** Humanity and Social Science & Management Courses, **AEC**–Ability Enhancement Courses. **UHV:** Universal Human Value Course.
L –Lecture, **T** – Tutorial, **P**- Practical/ Drawing, **S** – Self Study Component, **CIE:** Continuous Internal Evaluation, **SEE:** Semester End Examination.**TD**-Teaching Department, **PSB**: Paper Setting department

21KSK37/47 Samskrutika Kannada is for students who speak, read and write Kannada and **21KBK37/47** Balake Kannada is for non-Kannada speaking, reading, and writing students.

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC can be 04 and its Teaching–Learning hours (L : T : P) can be considered as (3 : 0 : 2) or (2 : 2 : 2). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated by only CIE (no SEE). However, questions from the practical part of IPCC shall be included in the SEE question paper. For more details, the regulation governing the Degree of Bachelor of Engineering /Technology (B.E./B.Tech.) 2021-22 may be referred.

21INT49Inter/Intra Institutional Internship: All the students admitted to engineering programs under the lateral entry category shall have to undergo a mandatory 21INT49 Inter/Intra Institutional Internship of 03 weeks during the intervening period of III and IV semesters. The internship shall be slated for CIE only and will not have SEE. The letter grade earned through CIE shall be included in the IV semester grade card. The internship shall be considered as a head of passing and shall be considered for vertical progression and for the award of degree. Those, who do not take up / complete the internship shall be declared fail and shall have to complete during subsequently after satisfying the internship requirements. The faculty coordinator or mentor shall monitor the students' internship progress and interact with them for the successful completion of the internship.

Non–credit mandatory courses (NCMC):

(A) Additional Mathematics I and II:

(1) These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.

(2) Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

(3) Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

(B) National Service Scheme/Physical Education (Sport and Athletics)/ Yoga:

(1) Securing 40 % or more in CIE,35 % or more marks in SEE and 40 % or more in the sum total of CIE + SEE leads to successful completion of the registered course.

(2) In case, students fail to secure 35 % marks in SEE, they have to appear for SEE during the subsequent examinations conducted by the University.

(3) In case, any student fails to register for NSS, PE or Yoga/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have not completed the requirements of the course. In such a case, the student has to fulfill the course requirements during subsequent semester/s to earn the qualifying CIE marks.

(4) Successful completion of the course shall be indicated as satisfactory in the grade card. Non-completion of the course shall be indicated as Unsatisfactory.

(5) These courses shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.

Ability Enhancement Course - III			
21EC381	LD (Logic Design) Lab using Pspice / MultiSIM	21EC383	LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM
21EC382	AEC (Analog Electronic Circuits) Lab	21EC384	LabVIEW Programming Basics

CALENDER OF EVENT

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IQAC
File I-11
2022-23 (Odd)
Rev: 00

CALENDAR OF EVENTS FOR THE ACADEMIC YEAR 2022-23 (Odd)

Date	Events
19-09-2022	Commencement of Classes for VII Semester
24-09-2022	NSS Foundation Day
02-10-2022	Gandhi Jayanthi
10-10-2022	Commencement of Classes for V Semester
24-10-2022 to 30-10-2022	Traffic Week
27-10-2022 to 29-10-2022	First Internal Assessment for VII Semester
31-10-2022	Feedback -I on Teaching-Learning for VII Semester
31-10-2022	National Integration Day
31-10-2022	Commencement of Classes for III Semester
01-11-2022	Kannad Rajyothsava
03-11-2022	Display of 1st Internal Assessment Marks and submission of Feedback-I of VII Semester to office
09-11-2022 to 18-11-2022	Environment Awareness Month
22-11-2022	World's Aids Day
26-11-2022	First Assignment Submission of III Semester (PCC + IPCC)
28-11-2022 to 30-11-2022	Second Internal Assessment for VII Semester & First Internal Assessment for III (PCC + IPCC) /V Semester
01-12-2022	Feedback –II on Teaching-Learning for VII Semester & Feedback – I on Teaching-Learning for III/V Semester
06-12-2022	Display of 2nd Internal Assessment Marks and submission of Feedback-II of VII Semester & Display of 1st Internal Assessment Marks and submission of Feedback-I of III/V Semester to office
10-12-2022	Human Rights Day
10-12-2022	Sports Day
23-12-2022 & 24-12-2022	First Lab Internal Assessment for III Semester (PCC+AEC)
26-12-2022 & 27-12-2022	Lab Internal Assessment for VII Semester
29-12-2022 to 31-12-2022	Third Internal Assessment for VII Semester & Second Internal Assessment for III (PCC + IPCC) /V Semester
31-12-2022	Last working day for VII Semester
02-01-2023	Feedback –II on Teaching-Learning for III/V Semester
05-01-2023	Display of Final IA Marks of VII Semester
05-01-2023	Display of 2nd Internal Assessment Marks and submission of Feedback-II of III/V Semester to office
07-01-2023	Second Assignment Submission of III Semester (PCC + IPCC)
12-01-2023	National Youth Day
15-01-2023	NSS Day
20-01-2023 & 21-01-2023	Lab Internal Assessment for V Semester
23-01-2023 to 25-01-2023	Third Internal Assessment for V Semester
26-01-2023	Republic Day
27-01-2023	Last working day for V Semester
30-01-2023 to 01-02-2023	Second Lab Internal Assessment for III Semester (PCC+IPCC+AEC)
31-01-2023	Display of Final IA Marks of V Semester
06-02-2023 to 08-02-2023	Third Internal Assessment for III Semester (PCC)
11-02-2023	Last working day for III Semester
14-02-2023	Display of Final IA Marks of III Semester

September-2022

S	M	T	W	T	F	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	

October-2022

S	M	T	W	T	F	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30	31					

04- Mahanavami, Ayudhapooja 05- Vijayadashami
24- Naraka Chaturdashi, 26- Balipadyami Deepavalli

Novemner-2022

S	M	T	W	T	F	S
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30			

01- Kannada Rajyothsava, 11- Kanakadasa Jayanti

December-2022

S	M	T	W	T	F	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

January-2023

S	M	T	W	T	F	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

14-Makara Sankranti, 26- Republic Day

February-2023

S	M	T	W	T	F	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

18- Mahashivaratri

19/9/22
Dr. B. V. Madiggond
Dean (Academics)

19/9
Dr. S. C. Kamate
Principal

Subject Title	**Transform Calculus, Fourier Series and Numerical Techniques**		
Subject Code	21MAT31	**IA Marks**	50
Number of Lecture Hrs /	04	**Exam Marks**	50
Total Number of Lecture Hrs	40	**Exam Hours**	03
		CREDITS – 03	

FACULTY DETAILS:		
Name: Dr. S. L. Patil	Designation: Asst. Professor	Experience: 14
No. of times course taught: 01	**Specialization:** Mathematics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics and Communication Engineering	II	Advanced Calculus & Numerical Methods

2.0 Course Objectives

Course Learning Objectives:

- To have an insight into Fourier series, Fourier transforms, Laplace transforms, Difference equations and Z- Transforms.
- To develop the proficiency in variation calculus and solving ODE's arising in engineering applications, using numerical methods.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

Course Code	Course Outcome	RBTL	POs
C201.1	Use Laplace transform and inverse Laplace transform in solving differential/ integral equation arising in network analysis, control systems and other fields of engineering.	L1,L2	1,2,3,12
C201.2	Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing and field theory.	L1, L2	1,2,3,12
C201.3	To use Fourier transforms to analyze problems involving continuous-time signals and to apply Z-Transform techniques to solve difference equations	L1, L2	1,2,3,12
C201.4	To solve mathematical models represented by initial or boundary value problems involving partial differential equations	L1, L2	1,2,3,12
C201.5	Determine the externals of functional using calculus of variations and solve problems arising in dynamics of rigid bodies and vibration analysis.	L1,L2,L3	1,2,3,12
Total Hours of instruction		**40**	

4.0 Course Content

Module-1: Laplace Transform:

Definition and Laplace transforms of elementary functions (statements only). Problems on Laplace's Transform of $e^{at}f(t), t^n f(t), \frac{f(t)}{t}$. Laplace transforms of Periodic functions (statement only) and unit-step function – problems.

Inverse Laplace Transform: Definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) and problems. Laplace transforms of derivatives, solution of differential equations.

Self-study: Solution of simultaneous first-order differential equations. **(8 Hours)**

Module -2: Fourier Series:

Introduction to infinite series, convergence and divergence. Periodic functions, Dirichlet's condition. Fourier series of periodic functions with period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.

Self-study: Convergence of series by D'Alembert's Ratio test and, Cauchy's root test. **(8 Hours)**

Module -3: Infinite Fourier Transforms and Z-Transforms

Infinite Fourier transforms definition, Fourier sine and cosine transforms. Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Problems. Difference equations, z-transform-definition, Standard z-transforms, Damping and shifting rules, Problems. Inverse z-transform and applications to solve difference equations. **(8 Hours)**

Self Study: Initial value and final value theorems, problems.

Module -4: Numerical Solution of Partial Differential Equations

Classifications of second-order partial differential equations, finite difference approximations to derivatives, Solution of Laplace's equation using standard five-point formula. Solution of heat equation by Schmidt explicit formula and Crank- Nicholson method, Solution of the Wave equation. Problems. **(8 Hours)**

Self Study: Solution of Poisson equations using standard five-point formula.

Module -5: Numerical Solution of Second-Order ODEs and Calculus of Variations

Second-order differential equations - Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). Calculus of Variations: Functionals, Euler's equation, Problems on extremals of functional. Geodesics on a plane, Variational problems. **(8 Hours)**

Self Study: Hanging chain problem

5.0 Relevance to future subjects

Sl. No.	Semester	Subject	Topics
01	Common to all	Common to all engineering Subjects	Signal and Analysis, Field Theory, Thermodynamics, Fluid Dynamics etc

6.0 Relevance to Real World

Sl. No	Real World Mapping
01	Numerical methods are used to solve engineering problems. For examples will be drawn from a variety of engineering problems, including heat transfer, vibrations, dynamics, fluid mechanics, etc.
02	Laplace transform are used in various areas of physics, electrical engineering, control engineering, optics, mathematics and signal processing. Laplace Transform is widely used by

	electronic engineers to solve quickly differential equations occurring in the analysis of electronic circuits
03	Fourier series is that very little information is lost from the signal during the transformation. The Fourier transform maintains information on amplitude, harmonics, and phase and uses all parts of the waveform to translate the signal into the frequency domain.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Calculus of Variations

8.0 Books Used and Recommended to Students

Text Books

1. B.S. Grewal, Higher Engineering Mathematics, 44th Edition 2018, Khanna Publishers.
2. E. Kreyszig: Advanced Engineering Mathematics, John Wiley & Sons, 10th Ed., 2016.
3. Srimanta Pal et al Engineering Mathematics, 3rd Edition, 2016, Oxford University Press.

Reference Books

1. V. Ramana: "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed.
2. Srimanta Pal & Subodh C. Bhunia: "Engineering Mathematics" Oxford University Press,3rd Reprint, 2016.
3. N.P Bali and Manish Goyal: "A textbook of Engineering Mathematics" Laxmi Publications, Latest edition.
4. C. Ray Wylie, Louis C. Barrett: "Advanced Engineering Mathematics" McGraw – Hill Book Co. New York, Latest ed.
5. Gupta C.B, Sing S.R and Mukesh Kumar: "Engineering Mathematic for Semester I and II", McGraw Hill Education (India) Pvt. Ltd 2015.
6. H. K. Dass and Er. Rajnish Verma: "Higher Engineering Mathematics" S. Chand Publication (2014).
7. James Stewart: "Calculus" Cengage publications,7th edition, 4th Reprint 2019.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

Web links and Video Lectures:

1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU Edusat Programme
5. VTU e-Shikshana Program
6. http://www.bookstreet.in.

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	+ Plus Magazine	https://plus.maths.org/issue44.
2	Mathematics Magazine	www.mathematicsmagazine.com

11.0 Examination Note

Assessment Details (both CIE and SEE)

The weight age of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination(SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of 20 Marks (duration 01 hour)
2. First test at the end of 5th week of the semester
3. Second test at the end of the 10th week of the semester
4. Third test at the end of the 15th week of the semester.

Two assignments each of 10 Marks

5. First assignment at the end of 4th week of the semester
6. Second assignment at the end of 9th week of the semester Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours)**
7. At the end of the 13th week of the semester The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks** (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject **(duration 03 hours)**

- The question paper will be set for 100 marks and marks scored will be proportionally scaled down to 50 marks
- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecturer	% of Portion
1	1	Definition, transforms of elementary functions & Properties	20
	2	Problems	
	3	Periodic function	
	4	Unit step function & Problems	
	5	Inverse Laplace Transforms	
	6	Convolution theorem	

	7	Solution of linear differential equations using Laplace Transforms	
	8	Problems	
2	9	Introduction to infinite series	20
	10	convergence and divergence	
	11	Introduction, Periodic functions, Dirichlet's conditions	
	12	Fourier series of periodic functions of period 2π & Problems	
	13	Fourier series of periodic functions of arbitrary period 2l & Problems	
	14	Fourier series of even & odd functions	
	15	Half range Fourier series & Problems	
	16	Practical harmonic analysis	
3	17	Introduction, Infinite Fourier transform	20
	18	Fourier sine transforms & Problems	
	19	Fourier cosine transforms & Problems	
	20	Inverse Fourier transforms & Problems	
	21	z-transform-definition & Standard z-transforms	
	22	Initial value and final value theorems (without proof) and problems	
	23	Inverse z-transform & Problems	
	24	Applications of z-transforms to solve difference equations	
4	25	Classifications of second-order partial differential equations	20
	26	Finite difference approximations to derivatives	
	27	Solution of Laplace's equation using standard five-point formula.	
	28	Problems.	
	29	Solution of heat equation by Schmidt explicit formula	
	30	Solution of heat equation by Crank- Nicholson method	
	31	Solution of the Wave equation	
	32	Problems.	
5	33	Numerical solution of second order ordinary differential equations	20
	34	Runge -Kutta method & Problems.	
	35	Milne's method & Problems.	
	36	Problems.	
	37	Calculus of Variations: Variation of function & Functional, variation problems	
	38	Euler's equation	
	39	Problems	
	40	Geodesics and problems	

13.0 Assignments

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity.	Book 1, of the reference list. Website of the Reference list
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

4	Assignment 4: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	10	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 QUESTION BANK

Module-1: Laplace Transform

1. Find the Laplace Transform of $sin2t\ sin3t$. & $sin^3 2t$.
2. Find $L\ (e^3 t sin2t)$ & $L(e^{4t}\ sin2t\ cost)$.
3. Find $L\left(\frac{1-e^t}{t}\right)$ & $L[\frac{cosat-cosbt}{t}]$
4. Using unit step function find LT of $f(t) = \begin{cases} \sin t, & 0 < t < \pi \\ \sin 2t, & \pi < t < 2\pi \\ \sin 3t, & t > 2\pi \end{cases}$
5. Express $f(t) = \begin{cases} \cos t, & 0 < t < \pi \\ \cos 2t, & \pi < t < 2\pi \\ \cos 3t, & t > 2\pi \end{cases}$ in terms unit step function & hence find LT
6. Evaluate $L[t^2 u(t-3)]$.
7. Find the inverse transform $\frac{s+2}{s^2-4s+13}$.
8. Find $L^{-1}\left(\frac{4s+5}{(s-1)^2(x+2)}\right)$
9. Find $L^{-1}\left(\frac{s}{s^4+4a^4}\right)$.
10. Find $L^{-1}\left(\frac{s}{(s^2+a^2)^2}\right)$.
11. Find $L^{-1}\left[\ log\ \frac{(s+1)}{(s-1)}\right]$
12. Find $L^{-1}\left[\frac{s}{(2s-1)(3s-1)}\right]$
13. Using the Convolution THM obtain the $L^{-1}\left[\frac{s}{(s^2+a^2)^2}\right]$.
14. Solve the differential equation $\frac{d^2y}{dx^2} - 3\frac{dy}{dx} + 2y\ = e^{3t}$ with $y(0) = 0 = y'(0)$, using LT
15. Solve the differential equation $y'' + 4y' + 3y = e^{-t}, y(0)\ = 1 =\ y'(0)$. Using LT

Module-2: Fourier series

1) Obtain a Fourier series to represent e^{-ax} from $(-\pi\ , x)$
2) Expand $f(x)\ =\ x\ sin\ x, 0\ <\ x\ <\ 2$, in a Fourier series.
3) For a function $f(x)$ defined by $f(x)\ =\ |x\ |, -\pi\ <\ x\ <\ \pi,$ obtain a Fourier series. Deduce that
   $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2} = \frac{\pi^2}{8}$
4. Find the Fourier series for the function $f(x) = \frac{\pi - x}{2}$ in $(0, 2\pi)$.
   Hence deduce that $\frac{\pi}{4} = 1 - \frac{1}{3} + \frac{1}{5} - - -$
5. Find the Fourier series to represent $f(x)\ =\ x + x^2$ from $x = -\pi$ to $x =\ \pi$ and deduce that
   $\frac{1}{1^2} - \frac{1}{2^2} + \frac{1}{3^2} - \frac{1}{4^2} = \frac{\pi^2}{12}$

6. Expand $f(x) = e^{-x}$ as a Fourier series in the interval $(-l, l)$
7. Obtain Fourier series for the function
   $f(x) = \begin{cases} \pi x, & 0 \le x \le 1 \\ \pi(2-x), & 1 \le x \le 2 \end{cases}$ and deduce that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2}$-------
8. Develop f(x) in Fourier series in the interval (-2, 2) if $f(x) = \begin{cases} 0, & -2 < x < 0 \\ 1, & 0 < x < 2 \end{cases}$
9. Find the half range cosine series for the function $f(x) = x^2$ in the range $0 \le x \le 1$
10. Find the complex form of the Fourier series of the periodic function $f(x) = cos\, ax$, in $-\pi < x < \pi$.
11. The following table gives the variation of periodic current over a period

t sec	0	T/6	T/3	T/2	2T/3	5T/6	T
A amp	1.98	1.30	1.05	1.30	-0.88	-0.25	1.98

Show that there is a direct current part of 0.75 amp in the variable current and obtain the amplitude of the first harmonic.

12. Obtain the Fourier expansion of $f(x) = 2x - x^2$ in $0 \le x \le 2$

13. Obtain the constant term and the coefficient of the first sine and cosine terms in the Fourier expansion of

y as given below.

x	0	1	2	3	4	5
y	9	18	24	28	26	20

Module-3: Infinite Fourier Transforms and Z-Transforms

1. Find the Fourier transform of
   $f(x) = \begin{cases} 1, & |x| < 1 \\ 0, & |x| < 1 \end{cases}$. Hence evaluate $\int_0^\infty \frac{sinx}{x} dx$
2. Find the Fourier transform of the function
   $f(x) = \begin{cases} x, & |x| \le \\ 0, & |x| > \alpha \end{cases}$. Where α is a positive constant?
3. Find the Fourier transform of $cosax^2$
4. Find the Fourier sine transform of e^{-ax}/x
5. Find the Fourier sine and cosine transform of $f(x) = \begin{cases} 1, & 0 \le x < a \\ 0, & x \ge a \end{cases}$
6. Find the finite Fourier sine and cosine transform of $f(x) = 2x, \quad 0 < x < 4$.
7. Find the cosine transform of $f(x) = \frac{1}{1+x^2}$
8. Find the Fourier sine transform of $e^{-|x|}$
9. Find the Fourier transform of $f(x) = \begin{cases} a^2 - x^2, & |x| < a \\ 0, & |x| > a \end{cases}$ and Evaluate $\int_0^\infty \frac{sinx - xcosx}{x^3} dx$.
10. Find the Fourier sine transform of $f(x) = \frac{e^{-ax}}{x}$, $a > 0$.
11. Find the Fourier cosine transform of $(x) = \begin{cases} x, & 0 < x < 1 \\ 2 - x, & 1 < x < 2 \\ 0, & x > 2 \end{cases}$.
12. Find the Fourier transform of $f(x) = e^{-|x|}$ and Evaluate $\int_0^\infty \frac{xsinmx}{1+x^2} dx$.
13. Find the Fourier transform of $f(x) = e^{-|x|}$ and Evaluate $\int_0^\infty \frac{xsinmx}{1+x^2} dx$.

14. P.T. $z_T(n^2) = \frac{z^2+z}{(z-1)^3}$
15. P.T. $z_T(n^3) = \frac{z^3+4z^2+2}{(z-1)^4}$
16. P.T. $z_T(cos\theta) = \frac{z(z-cos\theta)}{z^2-2zcos\theta+1}$
17. P.T. $z_T(sin\theta) = \frac{(zsin\theta)}{z^2-2zcos\theta+1}$
18. P.T. $z_T(a^n cosn\theta) = \frac{z(z-acos\theta)}{z^2-2azcos\theta+a^2}$
19. Find the Z-transform of $cos\ hn\theta$ & $sinhn\theta$.
20. Find the Z-transform of $(n\ +1)^2$
21. Using the inversion integral method find the inverse Z-transform of $\frac{3z}{(z-1)(z-2)}$
22. Solve $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ with $y_0 = y_n = 0$ using Z-transform
23. Solve the difference equation $y_{n+2} + 2y_{n+1} + y_n = n$ with $y_0 = y_n = 0$ using Z-Transform.
24. Obtain the z-transform of $cos\ n\theta$ and $sin\ n\theta$
25. Find the Inverse z-transform of $\frac{2z^2+3z}{(z+2)(z-4)}$.
26. If $\bar{u}(z) = \frac{2z^2+3z+12}{(z-1)^4}$, find the value of $u_0,\ u_1,\ u_2,\ u_3$.
27. Solve the difference equation $u_{n+2} + 6u_{n+1} + 9u_n = 2^n$, $u_0\ =\ u_1 = 0$.

Module -4: Numerical Solution of Partial Differential Equations

1. Solve $\frac{\partial u}{\partial t} = \frac{\partial^2 u}{\partial x^2}$ in $0 < x < 5,\ t \geq 0$ given that $u(x,0) = 20, u(0,t) = 0, u(5,t) = 100$.Compute u for thetime step with $h = 1$ by Crank Nicholson method.
2. Find the solution of the parabolic equation $u_{xx} = 2u_t$ when $u(0,t) = 0 =\ u(4,t) = 0$ and $u(x,0) =\ x(4-x)$, taking $h = 1$. Find the values up to $t = 5$.
3. Solve the equation $\frac{\partial^2 u}{\partial x^2} = \frac{\partial u}{\partial t}$ with the conditions $u(0,t) = 0, u(x,0) = x(1-x)$ and $u(1,t) = 0$. Assume $h = 0.1$. Tabulate u for $t = k, 2k$ and $3k$ choosing an appropriate value of k.
4. Solve the boundary value problem $u_{tt} = u_{xx}$ with the conditions $u(0,t) =\ u(1,t) = 0,\ u(x,0) = \frac{1}{2}x(1-x)$ and $u_t(x,0) = 0$, taking $h = k = 0.1$ for $0 \leq t \leq 0.4$. Compare your solution with the exact solution at $x = 0.5$ and $t = 0.3$.
5. Solve $y_{tt} = y_{xx}$ upto $t = 0.5$ with a spacing of 0.1 subject to $y(0,t) = 0, y(1,t) = 0, y_t(x,0) = 0$ and $y(x,0) = 10 + x(1-x)$.Solve the equation $u_{xx} + u_{yy} = 0$ for the following square mesh with boundary values as shown in Fig. Iterate until the maximum difference between the successive values at any point is less than 0.001.

Module -5: Numerical Methods and Calculus of Variation

1. Use R- K method to solve $y\ =\ xy'^2 -\ y^2$ for x = 0.2 correct to 4 decimal places. $y(0) = 1$ & $y'(0) = 0$
2. Evaluate $y(0.2)$ by RK method given that $y'' - x(y')^2 + y^2 = 0, y(0) = 1,\ y'(0) = 0$

3. Given $y'' - xy' - y = 0$ with the initial conditions y(0)=1, y'(0)=0. Compute y(0.2) and y'(0.2) by taking h=0.2 and using fourth order Runge Kutta method.
4. Obtain the solution of the equation $2\frac{d^2y}{dx^2} = 4x + \frac{dy}{dx}$ at the point $x = 1.4$ by applying Milne's method given that $y(1) = 2,\ y(1.1) = 2.2156,\ y(1.2) = 2.4649.\ y(1.3) = 2.7514, y'(1) = 2, y'(1.1) = 2.3178, y'(1.2) = 2.6725\ and\ y'(1.3) = 3.0657.$
5. Using R-K method of order four, solve $y'' = y + xy'$, y(0) = 1 , y'(0) to find $y(0.2)$ & $y'(0.2)$.
6. Show that the Geodesics on a plane are straight line.
7. Find the Geodesics on a right circular cylinder of radius a.
8. Find the extremals of the functional $\int_{x_0}^{x_1} \frac{(y'^2)}{x^3} dx$
9. Show that the shortest distance between any two points in a plane is a straight line.
10. Prove that Catenaries' is the curve which when rotated about a line generates a surface of minimum area.
11. Find the extremely of the functional $\int_0^{\pi}(y'^2 - y^2 + 4ycosx)dx;\ y(0) = 0 = y(\pi)$
12. Solve the variation problem $\delta\int_1^2(x^2(y')^2 + 2y(x+y))dx = 0, given\ y(1) = y(2) = 0$
13. Find the path on which a particle in the absence of friction will slide from one point to another in a shortest time under the action of gravity.
14. Find the curve passing through the point (x_1, y_1) and (x_2, y_2) which when rotated about the x axis gives the minimum surface area.
15. Find the curve on which the functional $\int_0^1(y'^2 + 12xy)\,dx$ with $y(0) = 0$ and $y(1) = 1$ can be extremised.

16.0 University Result

Examination	FCD (S+, S, A)	FC (B)	SC (C, D, E)	% Passing
Jan 2019	08	10	19	86.05
Jan 2018	09	04	20	89.18

Prepared by	Checked by		
Dr. S. L. Patil	Dr. S. L. Patil	**HOD**	**Principal**

Subject Title	**Digital System Design Using Verilog**		
Subject Code	21EC32	**IA Marks (20) +Assignments (10)**	30
Number of Lecture Hrs/Week /	03(L)	**Exam Marks**	20
Total Number of Lecture Hrs	40Theory + 13 Lab Slots	**Exam Hours**	03
CREDITS – 04			

FACULTY DETAILS:		
Name: Prof. D. B. Madihalli	**Designation:** Assistant Professor	**Experience:**15 years
No. of times course taught: 11	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to :

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of verilog HDL data flow and behavioral models for the design of digital systems.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Simplify Boolean functions using K-map & Quine-McCluskey minimization technique.	U	1,2,3,4,6,7,9,10, 11,12
CO2	Analyze and design MSI Components.	U	1,2,3,4,5,6,7,9,
CO3	Analyze the concepts of Flip Flops (SR, D, T & JK) and design the synchronous sequential circuits using flip flops.	U	1,2,3,4,5,6,7,9, 10,11,12
CO4	Understand the concept of verilog data flow description.	U	1,2,3,4,5,6,7,9, 10,11,12
CO5	Describe the verilog behavioral & structural description.	U	1,2,3,4,5,6,7,9, 10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Theory		
Modules	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
Module 1		
Principles of combinational logic: Definition of combinational logic, canonical forms, generation of switching equations from truth tables, karnaugh maps up to 4 variables, Quine-McCluskey minimization technique, Quine-McCluskey donot care terms.	08	L1,L2,L3
Module -2		
Logic Design with MSI Components and Programmable Logic Devices: Binary adders and subtractors, comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices.	08	L1,L2,L3
Module-3		
Flip-Flops and its applications: The master-slave flip-flops(pulse triggered flip-flops): SR flip-flops, JK flip-flops, characteristics equations, registers, binary ripple counters, synchronous binary counters, counters based on shift registers, design of synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	08	L1,L2,L3
Module-4		
Introduction to Verilog: Structure of verilog module, operators, data types, styles of description. **Verilog Data flow description:** Highlights of data flow description, structure of data flow description.	08	L1,L2,L3
Module-5		
Verilog Behavioral Description: Structure, variable assignment statement, sequential statements, loop statements, verilog behavioral description of multiplexers. **Verilog Structural Description:** Highlights of structural description, organization of structural description and structural description of ripple carry adder.	08	L1,L2,L3
Practical		
PART-A 1. To simplify the given boolean expressions and realize using verilog program. 2. To realize adder/subtractor (Full/Half) circuits using verilog data flow description. 3. To realize 4-bit ALU using verilog program. 4. To realize the following code converters using verilog behavioral description a) Gray to Binary & vice versa b) Binary to excess-3 & vice versa 5. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder. 6. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator. 7. To realize using verilog behavioral description: flip-flops: JK, SR, T and D. 8. To realize counters up/down (BCD and binary) using verilog behavioral description. **PART-B** 9. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.) 10. Verilog programs to interface relay or ADC to the FPGA/CPLD and demonstrate its working. 11. Verilog programs to interface DAC to the FPGA/CPLD for waveforms generation. 12. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.		2 Hours per Batch

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VI	Mini Project	HDL
02	VIII	Project Work	Embedded system & HDL based projects

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze digital circuits in real time applications
02	Integrated Circuits (Chip)
03	Model creation for analysis

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of problems.

8.0 Books Used and Recommended to Students

Text Books
1. Digital Logic Applications and Design by John M. Yarbough, Thomson Learning, 2001. 2. Digital Principles and Design by Donald D. Givone, McGraw Hill, 2002. 3. HDL Programming VHDL and Verilog by Nazeih M. Botros, 2009 reprint, Dreamtech Press.
Reference Books
1. Fundamentals of logic design by Charles H Roth Jr., Cengage Learning. 2. Logic Design by Sudhakar Samuel, Pearson / Sanguine, 2007. **3.** Fundamentals of HDL by Cyril P. R. Pearson/Sanguine 2010.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
1) https://nptel.co.in
2) http://www.slideshare.net/farohalolya/HDL
3) https://www.youtube.com

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Explorer	http://ieeexplore.ieee.org/Xplore/home.jsp
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Assessment Details both (CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC:

Two tests each of **20 marks (duration 01 hour)**

i) First test at the end of 5th week of the semester.
ii) Second test at the end of the 10th week of the semester.

Two assignments each of **10 marks**

i) First assignment at the end of 4th week of the semester.
ii) Second assignment at the end of 9th week of the semester.

Scaled down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for 30 marks.

CIE for the practical component of IPCC:

- On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks** shall be for the test conducted at the end of the semester.
- The CIE marks awarded in the case of the practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments write ups are added and scaled down to 15 marks.
- The laboratory test (duration 03 hours) at the end of the 15th week of the semester / after completion of all the experiments (whichever is early) shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled down marks of write up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC:

Theory SEE will be conducted by university as per the scheduled time table with common question papers for the course (duration 03 hours).

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub questions), should have a mix of topics under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE & SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks - 30) in the theory component and 08 (40% of maximum marks – 20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component

shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% Of Portion
1 Principles of Combinational Logic	1	Definition of combinational logic	Chalk and talk & YouTube Videos	20
	2	canonical forms	Chalk and talk	
	3	generation of switching equations from truth tables	Chalk and talk	
	4	karnaugh maps 2 variables	Chalk and talk	
	5	karnaugh maps 3 variables	Chalk and talk	
	6	karnaugh maps 4 variables	Chalk and talk	
	7	Quine-McCluskey 2,3 variables minimization technique	Chalk and talk	
	8	Quine-McCluskey 4 variables minimization technique & Quine-McCluskey do not care terms.	Chalk and talk	
2 Logic Design with MSI components and Programmable Logic Devices	9	Binary adders	Chalk and talk	20
	10	Binary Subtractors	Chalk and talk	
	11	Binary Comparators	Chalk and talk	
	12	Types of comparators	Chalk and talk	
	13	Decoders	Chalk and talk	
	14	Encoders	Chalk and talk	
	15	Multiplexers	Chalk and talk	
	16	Programmable Logic Devices	Chalk and talk & YouTube Videos	
3 Flip-Flops and Its Applications	17	The master-slave flip-flops(pulse triggered flip-flops)	Chalk and talk & YouTube Videos	20
	18	SR flip-flops	Chalk and talk	
	19	JK flip-flops, characteristics equations	Chalk and talk	
	20	registers, binary ripple counters,	Chalk and talk	
	21	synchronous binary counters,	Chalk and talk	
	22	counters based on shift registers,	Chalk and talk	
	23	Design of synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	Chalk and talk	
	24	Design of synchronous mod-n counter using clocked D and SR flip-flops.	Chalk and talk	
4 Introduction to Verilog and Verilog Data Flow Description	25	Introduction to Verilog	Chalk and talk & YouTube Videos	20
	26	Structure of verilog module	Chalk and talk	
	27	operators	Chalk and talk	
	28	data types	Chalk and talk	
	29	styles of description	Chalk and talk	
	30	Verilog Data flow description	Chalk and talk	
	31	Highlights of data flow description,	Chalk and talk	
	32	structure of data flow description	Chalk and talk	

5 Verilog Behavioral Description and Verilog Structural Description	33	Verilog Behavioral Description	Chalk and talk & YouTube Videos	20
	34	Structure, variable assignment statement	Chalk and talk	
	35	sequential statements, loop statements	Chalk and talk	
	36	verilog behavioral description of multiplexers	Chalk and talk	
	37	Verilog Structural Description:	Chalk and talk	
	38	Highlights of structural description	Chalk and talk	
	39	organization of structural description	Chalk and talk	
	40	structural description of ripple carry adder	Chalk and talk	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on canonical forms, K-map problems and QM method with & without do not care conditions problems.	Students study the Topics and will prepare for Final Exam.	Module-1 of the syllabus	3	Individual Activity	Text Book 1
2	Assignment 2: University Questions on arithmetic operators & programmable logic devices	Students study the Topics and will prepare for Final Exam.	Module-2 of the syllabus	6	Individual Activity.	Text Book 2
3	Assignment 3: University Questions on types of flip-flops, register & counters.	Students study the Topics and will prepare for Final Exam.	Module-3 of the syllabus	9	Individual Activity.	Text Book 2
4	Assignment 4: University Questions on operators, data types, data flow description, & its structure.	Students study the Topics and will prepare for Final Exam.	Module-4 of the syllabus	12	Individual Activity	Text Book 3
5	Assignment 5: University Questions on variable assignment & sequential statements, loop statements, organization & ripple carry adder of structural description	Students study the Topics and will prepare for Final Exam.	Module-5 of the syllabus	15	Individual Activity	Text Book 3

14.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

15.0 QUESTION BANK

Theory

Module – 1

1. Draw a model representing combinational circuits. Label the input & output variables. Write a general
2. expressions showing the input & output relationship.
3. 3. Explain combinational logic circuit with an examples.
4. 4. Explain the difference between combinational logic circuit & Sequential logic circuit
5. Construct a truth table & write the Boolean output equations for the following verbal problem statements-

a. A single output variable, Z, is to be true when the input variables a and b true and when b is false but a and c are true.

b. An output is to be true (logical 1) when the value of the inputs exceeds 3. The weighting for each input variable is as follows: w=3 x = 3 y =2 z = -1

5. Convert the following equations into their requested canonical forms:
   a. (SOP) X = ab + bc
   b. (POS) P = (w' + x) (y + z)
   c. (SOP) T = p(q + s)
   d. (SOP) R = L + M (NM + ML)
   e. (POS) U = r + s(t + r) + st
6. Simplify the following using Karnaugh maps:
   a. X = $a$bc + abc + abc
   b. Y= f(a, b, c) =Σ(1, 3, 5, 6, 7)
   c. T = $w$xy + wz + xy$z$
   d. P = f(w, x, y, z) = Σ(0, 2, 8, 10)
7. Convert the given Boolean function f(x, y, z) = [x + xz (y + z)] into maxterm canonical formula and hence highlight the importance of canonical formula.
8. Distinguish the prime implicants and essential prime implicants. Determine the same of the function f(w, x, y, z) = Σ m(0, 1, 4, 5, 9, 11, 13, 15)
9. F(a,b,c,d) = Σm(1,4,6,7,9,15) + Σd(3,5,11,13) Simplify using K-Map technique and implement by uisng gates.
10. Find the proper canonical form of the following expressions.
    i)Y = (a + b)(b + c) ii)F = A B + C D
11. Simply the following noncanonical expressions using Karnaugh maps:
    a. T = abcde + $a$bc$d$e + abcde + abcde
    b. P = vw + vwy + vwz
    c. G = yz + wxy + wxy + xyz
12. F(a,b,c,d) = ΠM(0,1,4,5,6,7,9,14) + Πd(13,15) Find maxterm simplified expression using K-Map technique and implement by using gates.
13. F(A,B,C,D) = A B D + ABC D + ABD + ABCD Simplify using K-Map and design its truth table. Also write its verilog program.
14. F = Σm(6,7,9,10,13)+ Σd(4,5,11,15) Simplify using K-Map and implement using NAND gate.
15. F(a,b,c,d) = (a + b) (b + c) Simplify using K-Map and design its truth table. Also write its verilog program.
16. F = ΠM (6,7,9,10,13)+ Πd(4,5,11,15) Simplify using K-Map and implement using NOR gate.
17. Find the canonical formula in POS form of the following expressions.

i)Y = A(A+B+C) ii)F = (P+*Q*) (P+R)

18. Using Quine – Mcluskey method and prime implicant reduction table, obtain the minimal sum expression for the Boolean function f(w, x, y, z) = Σ m(1, 4, 6, 7, 8, 9, 10, 11, 15).

19. Obtain the minimal product of the following Boolean functions using QM technique: f(w, x, y, z) = Σ m(1, 5, 7, 10, 11) + dc(2, 3, 6, 13)

Module -2

1. Shortly explain the decoder.
2. Design 4:16 decoder using two 3:8 decoder.
3. Design 5:32 decoder using one 2:4 & four 3:8 decoder IC's.
4. Explain realization of multiple output function using Binary decoder.
5. Implement following function using 3:8 decoder – f1(A,B,C) = m(1,4,5,7) and f2(A,B,C) = M(2,3,6,7).
6. Design combinational circuit of BCD to 7 segment display using decoder.
7. Write short note on – encoder.
8. Design keypad interface to digital system using 10 lines to BCD encoder.
9. Design octal to binary encoder.
10. Briefly explain priority encoder.
11. Design 32:5 priority encoder using four 74LS148 & gates.
12. Implement full adder & full substractor using decoder & write its truth table.
13. Write short note on – multiplexer and de-multiplexer.
14. Design 32:1 MUX using two 74LS150 ICs.
15. Design 32:1 MUX using four 8:1 MUX & 2:4 decoder.
16. Implement following functions using 4:1, 8:1 & 16:1 MUX - f1(A,B,C,D) = Σ m(0,1,2,4,6,9,12,14) and f2(A,B,C,D) =Σ m(0,1,3,4,8,9,15).
17. Implement following expression – F(A, B, C, D) = ABD + ACD + BCD + ACD using 8:1 MUX.
18. Construct 8:1 MUX using 2:1 MUX.
19. Implement full adder & full substractor using DeMUX.
20. Explain the concept of carry look ahead adder. Design 4-bit carry look ahead circuit.
21. Design 2-bit comparator.
22. Explain full adder & full substractor circuit.
23. Explain the programmable logic devices

Module -3

1. Explain the difference between combinational & sequential circuits.
2. Explain the difference between synchronous & asynchronous sequential circuits.
3. Explain the operation of SR Flip Flop.
4. Explain the working of switch Debouncer using SR latch.
5. Explain SR latch using NOR gate & Gated SR latch using NOR & NAND gate.
6. Explain Characteristics of SR Latch & its state Transition Diagram.
7. Explain the race around condition in detail. How it is eliminated?
8. Draw the master slave SR flip – flop. Explain flip-flop action during control signal & also give the truth table.
9. Draw & explain master slave JK flip-flop.
10. Explain JK , T & D-flip-flop.
11. Draw & explain edge triggered flip-flop.
12. Convert SR flip flop to JK flip flop.
13. Explain Left shift serial in serial out register with D flip flop.
14. Explain serial in parallel out shift register.
15. Explain parallel in serial out shift register.
16. Explain Ring counter & Johnson Counter.
17. Explain binary ripple counters.
18. Explain synchronous binary counter.

Module – 4

1. Explain the introduction to verilog.
2. Explain the types of data.
3. Explain the styles of description.
4. Explain the data flow description.
5. Explain the structure of the verilog module.
6. Explain the verilog operators.
7. Explain the data flow description.

Module – 5

1. Explain the verilog behavioral description of multiplexer.
2. Explain the verilog structural description of 4 bit ripple carry adder.
3. Explain the structure of verilog behavioral description.
4. Explain variable assignment statement.
5. Explain sequential statements.
6. Explain the loop statements.
7. Explain the verilog structural description.
8. Explain the organization of structural description.

Prepared by	Checked by		
Prof. D. B. Madihalli	Dr. S. S. Ittannavar	HOD	Principal

Subject Title	**Digital System Design Using Verilog Lab**		
Subject Code	21EC32	**Laboratory work (20)**	20
Number of Lecture Hrs/Week /	2(P)	**Exam Marks**	50
Total Number of Lecture Hrs	13 Lab Slots	**Test Hours**	03
CREDITS – 04			

FACULTY DETAILS:		
Name: Prof. D. B. Madihalli	**Designation:** Assistant Professor	**Experience:**15 years
No. of times course taught: 01	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesise the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.	U	1,2,3,4,6,7,9, 10,11,12
CO2	Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.	U	1,2,3,4,5,6,7, 9,10,11,12
CO3	Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.	U	1,2,3,4,5,6,7, 9,10,11,12
CO4	Interface the hardware to the programmable chips and obtain the required output.	U	1,2,3,4,5,6,7, 9,10,11,12
CO5	Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.	U	1,2,3,4,5,6,7, 9,10,11,12
Total Hours of instruction		**24**	

4.0 Course Content

Practical		
Experiments	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
PART-A 13. To simplify the given boolean expressions and realize using verilog program.	02	L3
14. To realize adder/subtractor (Full/Half) circuits using verilog data flow description.	02	L3
15. To realize 4-bit ALU using verilog program.	02	L3
16. To realize the following code converters using verilog behavioral description b) Gray to Binary & vice versa b) Binary to excess-3 & vice versa	02	L3
17. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder.	02	L3
18. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator.	02	L3
19. To realize using verilog behavioral description: flip-flops: JK, SR, T and D.	02	L3
20. To realize counters up/down (BCD and binary) using verilog behavioral description.	02	L3
PART-B	02	L3
21. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.)	02	L3
22. Verilog programs to interface relay or ADC to the FPGA/CPLD and demonstrate its working.	02	L3
23. Verilog programs to interface DAC to the FPGA/CPLD for waveforms generation.	02	L3
24. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.	02	L3

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VI	Mini Project	HDL
02	VIII	Project Work	Embedded system.

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze digital circuits in real time applications

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of programs

8.0 Books Used and Recommended to Students

4. Lab Manual

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
4) https://nptel.co.in

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Explorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

CIE for the practical component of IPCC:

- On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks** shall be for the test conducted at the end of the semester.
- The CIE marks awarded in the case of the practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments write ups are added and scaled down to 15 marks.
- The laboratory test (duration 03 hours) at the end of the 15th week of the semester / after completion of all the experiments (whichever is early) shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled down marks of write up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

12.0 Course Delivery Plan

Experiments	% of portion
PART-A 1. To simplify the given boolean expressions and realize using verilog program.	8
2. To realize adder/subtractor (Full/Half) circuits using verilog data flow description.	16
3. To realize 4-bit ALU using verilog program.	25
4. To realize the following code converters using verilog behavioral description c) Gray to Binary & vice versa b) Binary to excess-3 & vice versa	33

5. To realize using verilog behavioral description: 8:1 mux, 8:3 encoder, Priority encoder.	42
6. To realize using verilog behavioral description: 1:8 mux, 3:8 decoder, 2-bit comparator.	50
7. To realize using verilog behavioral description: flip-flops: JK, SR, T and D.	58
8. To realize counters up/down (BCD and binary) using verilog behavioral description.	67
PART-B	
9. Verilog program to interface stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps.)	75
10. Verilog programs to interface relay or ADC to the FPGA/CPLD and demonstrate its working.	84
11. Verilog programs to interface DAC to the FPGA/CPLD for waveforms generation.	92
12. Verilog programs to interface switches and LEDs to the FPGA /CPLD and demonstrate its working.	100

13.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

14.0 VIVA BANK

1. HDL stands for_____.
2. VHDL stands for_____.
3. Explain the structure of Verilog module.
4. Explain Verilog Ports.
5. List the logical operators. Explain any one with example.
6. List the Relational operators. Explain any one with example.
7. List the Arithmetic operators. Explain any one with example.
8. Explain Shift and Rotate operators.
9. What is Data type?
10. Explain the Verilog Data types.
11. Compare VHDL and Verilog.
12. If A and B are two unsigned variables, with A=1100 and B=1001, find the value of

The following expressions:

a. (A AND B) b. (A ^ B) c. (A & B) d. (A NOR B) e. (A && B) f. !(B) g. ~|(A) h. A >>1 i. B ror 2

13. What do you mean concurrent statements?
14. Draw the simulation wave form for 2x1 MUX.
15. What is logic synthesis?
16. Explain Signal declaration and assignment statements.
17. What is sensitivity list?
18. Explain the structure of PROCEDURE in Verilog.
19. Explain the structure of TASKS in Verilog.

20. Explain the structure of FUNCTIONS in Verilog.
21. Which IDE is used for Verilog code development?
22. How many windows get open when you open the Xilinx Project Navigator?
23. FPGA stands for_____.
24. JTAG stands for_____.
25. Which simulator is used in Lab.

Prepared by	Checked by		
Prof. D. B. Madihalli	Dr. S. S. Ittannavar	HOD	Principal

Subject Title	**Basic Signal Processing**		
Subject Code	21EC33	**IA Marks (20) +Assignments (10) + CIE Marks for Laboratory Component of IPCC**	50
Number of Lecture Hrs/Week /	03(L)	**Exam Marks (appearing for)**	50 (100)
Total Number of Lecture Hrs	40 Theory + 13 Lab Slots	**Exam Hours**	03
CREDITS – 04			

FACULTY DETAILS:		
Name: Dr. S. S. Ittannavar	**Designation:** Assistant Professor	**Experience:**10 years
No. of times course taught: 01	**Specialization:** Digital Signal Processing	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Understand the basics of Linear Algebra	U	1,2,3,4,5,6,7,8,9 ,10,11,12
CO2	Analyse different types of signals and systems	U	1,2,3,4,5,6,7,8,9
CO3	Analyse the properties of discrete time signals & systems	U	1,2,3,4,5,6,7,8,9 ,10,11,12
CO4	Analyse discrete time signals & systems using Z transforms	U	1,2,3,4,5,6,7,8,9 ,10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1		
Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram-Schmidt Orthogonalization procedure **(Refer Chapters 2 and 3 of Text 1)**	**08**	**L1, L2,L3**
Module -2		
Eigen values and Eigen vectors: Review of Eigen values and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 1)**	**08**	**L1, L2,L3**
Module-3		
Introduction and Classification of signals: Definition of signal and systems with examples, Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions **Basic Operations on signals:** Amplitude scaling, addition, multiplication, time scaling, time shift and time reversal. Expression of triangular, rectangular and other waveforms in terms of elementary signals **System Classification and properties:** Linear-nonlinear, Time variant - invariant, causal-noncausal, static-dynamic, stable-unstable, invertible. **(Text 2) [Only for Discrete Signals & Systems]**	**08**	**L1, L2,L3**
Module-4		
Time domain representation of LTI System: Impulse response, convolution sum. Computation of convolution sum using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular. **LTI system Properties in terms of impulse response:** System interconnection, Memory less, Causal, Stable, Invertible and Deconvolution and step response **(Text 2) [Only for Discrete Signals & Systems]**	**08**	**L1, L2,L3**
Module-5		
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform by partial fraction, Causality and stability, Transform analysis of LTI systems. **(Text 2)**	**08**	**L1, L2, L3**

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	V	Digital Signal Processing	Linear filtering
02	VI	Mini Project	DSP
03	VIII	Project Work	DSP based projects

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze different signals in real time applications
02	Model creation for analysis

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of problems.

8.0 Books Used and Recommended to Students

Text Books

1. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327
2. Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN9971-51- 239-4.

Reference Books

1. Michael Roberts, "Fundamentals of Signals & Systems",2nd edition, Tata McGraw-Hill, 2010, ISBN978-0- 07-070221-9.
2. Alan V Oppenheim, Alan S WiIlsky and S Hamid Nawab, "Signals and Systems" Pearson Education Asia / PHI, 2"" edition, 1997. Indian Reprint 2002.
3. H P Hsu, R Ranjan, "Signals and Systems", Schaum's outlines, TMH, 2006.
4. B P Lathi, "Linear Systems and Signals", Oxford University Press, 2005.
5. Ganesh Rao and Satish Tunga, "Signals and Systems", Pearson/Sanguine.
6. Seymour Lipschutz, Marc Lipson, "Schaums Easy Outline of Linear Algebra", 2020.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

Video lectures on Signals and Systems by Alan V Oppenheim
Lecture 1, Introduction | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube
Lecture 2, Signals and Systems: Part 1 | MIT RES.6.007 Signals and Systems, Spring 2011 - YouTube
NPTEL video lectures signals and system:
https://www.youtube.com/watch?v=7Z3LE5uM-6Y&list=PLbMVogVj5nJQQZbah2uRZIRZ_9kfoqZyx
Video lectures on Linear Algebra by Gilbert Strang
5) https://www.youtube.com/watch?v=ZK3O402wf1c&list=PL49CF3715CB9EF31D&index=1

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Explorer	http://ieeexplore.ieee.org/Xplore/home.jsp
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Assessment Details both (CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of IPCC:

Two tests each of **20 marks (duration 01 hour)**

iii) First test at the end of 5th week of the semester.

iv) Second test at the end of the 10th week of the semester.

Two assignments each of **10 marks**

iii) First assignment at the end of 4th week of the semester.

iv) Second assignment at the end of 9th week of the semester.

Scaled down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for 30 marks.

CIE for the practical component of IPCC:

- On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks** shall be for the test conducted at the end of the semester.
- The CIE marks awarded in the case of the practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments write ups are added and scaled down to 15 marks.
- The laboratory test (duration 03 hours) at the end of the 15th week of the semester / after completion of all the experiments (whichever is early) shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled down marks of write up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC:

Theory SEE will be conducted by university as per the scheduled time table with common question papers for the course (duration 03 hours).

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub questions), should have a mix of topics under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE & SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks - 30) in the theory component and 08 (40% of maximum marks – 20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% of Portion
1. Vector Spaces	1	Vector spaces and Null subspaces,	Chalk and talk	20
	2	Rank and Row reduced form, Independence,	Chalk and talk	
	3	Basis and dimension, Dimensions of the four subspaces	Chalk and talk	
	4	Rank-Nullity Theorem,	Chalk and talk	
	5	Linear Transformations Orthogonality:	Chalk and talk	
	6	Orthogonal Vectors and Subspaces, Projections	Chalk and talk	
	7	Least squares, Orthogonal Bases	Chalk and talk	
	8	Gram-Schmidt Orthogonalization procedure	Chalk and talk	
2. Eigen Values and Eigen Vectors	9	Review of Eigen values and Diagonalization of a Matrix	Chalk and talk	20
	10	Problems on Eigen Values	Chalk and talk	
	11	Problems on Diagonalization of a matrix	Chalk and talk	
	12	Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition.	Chalk and talk	
	13	Special Matrices (Positive Definite, Symmetric) Problems	Chalk and talk	
	14	Problems on matrices	Chalk and talk	
	15	Properties on Matrices	Chalk and talk	
	16	Singular Value Decomposition	Chalk and talk	
3. Introduction and Classification of signals Basic Operations on signals System Classification and properties	17	Definition of signal and systems with examples,	Chalk and talk	20
	18	Elementary signals/Functions: Exponential, sinusoidal, step, impulse and ramp functions	Chalk and talk	
	19	Amplitude scaling, addition, multiplication	Chalk and talk	
	20	Problems on basic operations on signals	Chalk and talk	
	21	Time scaling, time shift and time reversal.	Chalk and talk	
	22	Problems on sketching of signals	Chalk and talk	
	23	Expression of triangular, rectangular and other waveforms in terms of elementary signals	Chalk and talk	
	24	Linear-nonlinear, Time variant -invariant, causal-non causal, static-dynamic, stable-unstable, invertible.	Chalk and talk	
4. Time domain representation of LTI System, LTI system Properties in terms of impulse response	25	Impulse response, convolution sum.	Chalk and talk	20
	26	Computation of convolution sum using graphical method for unit step and unit step.	Chalk and talk	
	27	Computation of convolution sum using graphical method for unit step and exponential.	Chalk and talk	
	28	Computation of convolution sum using graphical method for exponential and exponential.	Chalk and talk	
	29	Computation of convolution sum using graphical method for unit step and rectangular	Chalk and talk	
	30	Computation of convolution sum using graphical method for rectangular and rectangular.	Chalk and talk	
	31	System interconnection, Memory less, Causal, Stable, Invertible	Chalk and talk	
	32	De convolution and step response	Chalk and talk	

5. The Z-Transforms	33	Z transform, properties of the region of convergence	Chalk and talk	20
	34	Problems on Z transform	Chalk and talk	
	35	Properties of the Z-transform	Chalk and talk	
	36	Problems on Properties of the Z-transform	Chalk and talk	
	37	Inverse Z-transform by partial fraction	Chalk and talk	
	38	Problems on Inverse Z-transform	Chalk and talk	
	39	Causality and stability, Transform analysis of LTI systems.	Chalk and talk	
	40	Problems on transform analysis of LTI systems	Chalk and talk	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on vector spaces, Eigen values & Eigen vectors, Introduction and Classification of signals	Students study the Topics and will prepare for Final Exam.	Module-1, 2 & 3 of the syllabus	9	Individual Activity	Text Book 1 & 2
2	Assignment 2: University Questions on Basic Operations on signals System Classification and properties, Time domain representation of LTI System, LTI system Properties in terms of impulse response, The Z-Transforms	Students study the Topics and will prepare for Final Exam.	Module-3,4 & 5 of the syllabus	12	Individual Activity.	Text Book 2

14.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

15.0 QUESTION BANK

Theory

Module – 1

1. Describe the column space and the null space of the following matrices.

   (i) $A = \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix}$ (ii) $B = \begin{bmatrix} 0 & 0 & 3 \\ 1 & 2 & 3 \end{bmatrix}$
2. Determine whether the vectors (1, 3, 2), (2, 1, 3) and (3, 2, 1) are linearly dependent or independent.
3. Define Vector Subspaces and explain the four fundamental subspaces.
4. Determine whether or not each of the following forms a basis in $\mathbb{R}3$. $x1$ = (2, 2, 1), $x2$ = (1, 3, 7) and $x3$ = (1, 2, 2).

Module -2

1. Find the eigen values and eigen vectors of matrix A.

$$A = \begin{bmatrix} 1 & 4 \\ 2 & 3 \end{bmatrix}$$

2. Factor the matrix A into $A = X\Lambda X^{-1}$ using diagonalization and hence find A^3.

$$A = \begin{bmatrix} 1 & 2 \\ 0 & 3 \end{bmatrix}$$

3. What is a positive definite matrix? Mention the methods of testing positive definiteness.
4. If a 4 × 4 matrix has det(A) = 1 2 then find the following. (i) $det\ (2A)$ (ii) det($-A$) (iii) det(A^2) (iv) det (A^{-1})

Module -3

1. Distinguish between i) Even and Odd Signals ii) Periodic and nonperiodic signals
2. Determine whether the following signals are periodic, if periodic determine the fundamental period. i) x(t) = cos2t + sin3t ii)x[n] = sin2n
3. Determine whether the system y(t) = x(n^2) is i) Linear ii) Time-invarient iii) Memory iv) Causal v) Stable
4. Determine and sketch the even and odd components of the following signals:

$$\text{(i)} \qquad x[n] = \begin{cases} -2 + n^2, & -1 \le n \le 3 \\ 0, \text{otherwise} \end{cases}$$

5. Sketch and determine the energy of the following signals: x[n]=− u[n−1]+u[n−5]

Module – 4

1. Consider an LTI system with input x(n) & unit impulse response h(n) given below, Compute y(n). x(n) = 2n u(-n); & h(n) = u(n)
2. Find the step response for the LTI system represented by impulse response i) h(n) = u(n) ii) h(n) = $(1/2)^n$ u(n)
3. Determine whether the following system represented by input-output relation is stable and causal: y[n]=x[n+1]+x[n]+x[n−1].
4. Given x[n]=α^nu[n] and h[n]=β^n u[n−1], obtain y[n] =x[n] *h[n].
5. Show that distributive and associative laws hold good with respect to convolution operator in discrete-time domain.

Module – 5

1. What is Region of Convergence (ROC) of Z-Transform? Mention its properties.
2. State and prove the following properties of Z-transform: (i) Time-reversal (ii) Multiplication by exponential function
3. Find the Z-transform of x[n]=0.5^nu[n]+2^nu[−n−1].
4. A stable and causal LTI system is described by the difference equation: y[n]+0.25y[n−1]−0.125 y[n−2]=−2x[n]+1.25 x[n−1]. Find the system impulse response.
5. An LTI system has impulse response h[n]=0.5^nu[n]. Determine the input to the system if the output is given by y[n]=0.5^nu[n]+$(-0.5)^n$u[n]

Prepared by	Checked by		
Dr. S. S. Ittannavar	Prof. D. B. Madihalli	HOD	Principal

Subject Title	**Basic Signal Processing Lab**		
Subject Code	21EC33	**Conduction of experiments (15)+ Laboratory Test (5)**	20
Number of Lecture Hrs/Week /	2(P)	**Exam Marks**	50
Total Number of Lecture Hrs	13 Lab	**Test Hours**	03
CREDITS – 02			

FACULTY DETAILS:		
Name: Dr. S.S.Ittannavar	**Designation:** Assistant Professor	**Experience:**10 years
No. of times course taught: 01	**Specialization:** Digital Signal Processing	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Basic Electronics

2.0 Course Objectives

This course will enable students to:

Preparation: To prepare students with fundamental knowledge/ overview in the field of Signal Processing with Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.

Core Competence: To equip students with a basic foundation of Signal Processing by delivering the basics of quantitative parameters for Matrices & Linear Transformations, the mathematical description of discrete time signals and systems, analyzing the signals in time domain using convolution sum, classifying signals into different categories based on their properties, analyzing Linear Time Invariant (LTI) systems in time and transform domains.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Understand the basics of Linear Algebra	U	1,2,3,4,6,7,9,10,11,12
CO2	Analyze different types of signals and systems	U	1,2,3,4,5,6,7,9,10,11, 12
CO3	Analyze the properties of discrete time signals & systems	U	1,2,3,4,5,6,7,9,10,11, 12
CO4	Analyze discrete time signals & systems using Z transforms	U	1,2,3,4,5,6,7,9,10,11, 12
Total Hours of instruction		**24**	

4.0 Course Content

Practical Component of IPCC		
Experiments	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
1. a. Program to create and modify a vector (array). b. Program to create and modify a matrix.	02	L3
2. Programs on basic operations on matrix	02	L3
3. Program to solve system of linear equations.	02	L3
4. Program for Gram-Schmidt Orthogonalization.	02	L3
5. Program to find Eigen value and Eigen vector.	02	L3
6. Program to find Singular value decomposition.	02	L3
7. Program to generate discrete waveforms.	02	L3
8. Program to perform basic operation on signals.	02	L3
9. Program to perform convolution of two given sequences.	02	L3
a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. c. Program to perform verification of associative property of convolution.	02	L3
11. Program to compute step response from the given impulse response.	02	L3
12. Programs to find Z-transform and inverse Z-transform of a sequence.	02	L3

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	V	Digital Signal Processing	Linear filtering
02	VI	Mini Project	DSP
03	VIII	Project Work	DSP based projects

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze different signals in real time applications
02	Model creation for analysis

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Solving different types of programs

8.0 Books Used and Recommended to Students

5. Lab Manual

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

6) https://nptel.co.in

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Explorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

CIE for the practical component of IPCC:

- On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks** shall be for the test conducted at the end of the semester.
- The CIE marks awarded in the case of the practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments write ups are added and scaled down to 15 marks.
- The laboratory test (duration 03 hours) at the end of the 15th week of the semester / after completion of all the experiments (whichever is early) shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled down marks of write up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

12.0 Course Delivery Plan

Experiments	% of portion
1. a. Program to create and modify a vector (array). b. Program to create and modify a matrix.	8
2. Programs on basic operations on matrix	16
3. Program to solve system of linear equations.	25
4. Program for Gram-Schmidt Orthogonalization.	33
5. Program to find Eigen value and Eigen vector.	42
6. Program to find Singular value decomposition.	50
7. Program to generate discrete waveforms.	58
8. Program to perform basic operation on signals.	67
9. Program to perform convolution of two given sequences.	75
10. a. Program to perform verification of commutative property of convolution. b. Program to perform verification of distributive property of convolution. c. Program to perform verification of associative property of convolution.	84
11. Program to compute step response from the given impulse response.	92
12. Programs to find Z-transform and inverse Z-transform of a sequence.	100

13.0 University Result

Examination	S+	S	A	B	C	D	E	F	% of passing
First Time Introduced	-	-	-	-	-	-	-	-	-

14.0 VIVA QUESTIONS

1. Define Signal and system.
2. What are the major classifications of the signal?
3. Define discrete time signals and classify them.
4. Define continuous time signals and classify them.
5. Define unit ramp signal.
6. Define periodic signal. and non periodic signal.
7. Define even and odd signal ?
8. Define Energy and power signal.
9. Define unit pulse function.
10. Define continuous time complex exponential signal.
11. Define a causal and non causal system
12. Define memory and memoryless system.
13. Why CT signals are represented by samples.
14. What are the effects aliasing.
15. State the methods to find inverse Z transform.
16. State multiplication property in relation to Z transform.
17. Define impulse response of a DT system.
18. What are the properties of convolution.

Prepared by	Checked by		
Dr. S. S. Ittannavar	Prof. D. B. Madihalli	HOD	Principal

Subject Title	**Analog Electronic Circuits**		
Subject Code	**21EC34**	**IAMarks (20+20+20) +Assignments (10+10) + GD/Quiz/Seminar (20)**	50(100)
Number of Lecture Hrs/Week /	03	**Exam Marks (appearing for)**	50 (100)
Total Number of Lecture Hrs	40	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. D M Kumbhar	**Designation:** Assistant Professor	**Experience :Teach- 15** years (Ind 07years)
No. of times course taught: 01	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	I & II	Basic electrical & electronics subjects

2.0 Course Objectives

This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET..

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
C204.1	Understand the characteristics of BJT sand FETs for switching and amplifier circuits.	U	1,2,3,4,5,6,7,8 ,9,10,11,12
C204.2	Design and analyze FET amplifiers and oscillators with different circuit configurations and biasing conditions.	U	1,2,3,4,5,6,7,8 ,9,10,11,12
C204.3	Understand the feedback topologies and approximations in the design of amplifiers and oscillators.	U	1,2,3,4,5,6,7,8 ,9,10,11,12
C204.4	Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.	U	1,2,3,4,5,6,7,8 ,9,10,11,12
C204.5	Understand the power electronic device components and its functions for basic power electronic circuits.	U	1,2,3,4,5,6,7,8 ,9,10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1		
BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage- divider bias), Biasing using a collector to base feedback resistor. **Small signal operation and Models:** Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model. **MOSFETs:** Biasing in MOS amplifier circuits: FixingVGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.	**08**	**L1, L2,L3**
Module -2		
MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower. **MOSFET internal capacitances and High frequency model:** The gate capacitive effect, Junction capacitances, High frequency model. **Frequency response of the CS amplifier:** The three frequency bands, high frequency response, Low frequency response. **Oscillators:** FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation)	**08**	**L1, L2,L3**
Module-3		
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (QualitativeAnalysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier.	**08**	**L1, L2,L3**
Module-4		
Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC – Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators.	**08**	**L1, L2,L3**
Module-5		
Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit.	**08**	**L1, L2, L3**

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII/VIII	Project Work	All Modules
02	V	Analog Communication	AM. FM. PM, Noise Analysis
02	VI	Digital Communication	Digital Modulation schemes, Spread Spectrum techniques

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Design of electronic circuits for different applications.
02	Hobby/Mini projects
03	Home appliances/ controlling of equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Assembly Application

8.0 Books Used and Recommended to Students

Text Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth CSmith, 6th Edition, Oxford, 2015. ISBN: 978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. M D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897.

Reference Books

1. Electronic Devices and Circuit Theory, Robert L Boylestad and Louis Nashelsky, 11th Edition, Pearson Education, 2013, ISBN: 978-93-325-4260-0.
2. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, John Weily, 2015, ISBN 978-81-265-7135-2
3. J.Millman&C.C.Halkias—Integrated Electronics, 2nd edition, 2010, TMH. ISBN 0-07-462245-5

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

7) https://nptel.co.in
8) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details both (CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester Two

assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the Cos and Pos for **20Marks** (**Duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50marks**

(To have less stressed CIE, the portion of the syllabus should not be common/repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled time table, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for20marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored out of 100 shall be proportionally reduced to 50marks.

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	Teaching Method	% Of Portion
1	1	**BJT Biasing:** Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage- divider bias)	Chalk and talk, PPT	20
	2	Biasing using a collector to base feedback resistor.	Chalk and talk, PPT	

	3	**Small signal operation and Models:** Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain	Chalk and talk, PPT	
	4	Separating the signal and the DC quantities, The hybrid Π model, The T model	Chalk and talk, PPT	
	5	**MOSFETs:** Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG	Chalk and talk, PPT	
	6	Drain to Gate feedback resistor.	Chalk and talk, PPT	
	7	Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain	Chalk and talk, PPT	
	8	Small signal equivalent circuit models, transconductance, The T equivalent circuit model.	Chalk and talk, PPT	
2	9	Basic configurations, characterizing amplifiers,	Chalk and talk, PPT	20
	10	CS amplifier with and without source resistance RS	Chalk and talk, PPT	
	11	Source follower	Chalk and talk, PPT	
	12	The gate capacitive effect, Junction capacitances, High frequency model	Chalk and talk, PPT	
	13	The three frequency bands, high frequency response	Chalk and talk, PPT	
	14	Low frequency response.	Chalk and talk, PPT	
	15	FET based Phase shift oscillator	Chalk and talk, PPT	
	16	LC and Crystal Oscillators	Chalk and talk, PPT	
3	17	General feedback structure, Properties of negative feedback	Chalk and talk, PPT	20
	18	The Four Basic Feedback Topologies	Chalk and talk, PPT	
	19	The series-shunt, series-series amplifiers	Chalk and talk, PPT	
	20	shunt-shunt and shunt-series amplifiers	Chalk and talk, PPT	
	21	Introduction, Classification of output stages, Class A output stage	Chalk and talk, PPT	
	22	Class B output stage: Transfer Characteristics	Chalk and talk, PPT	
	23	Power Dissipation, Power Conversion efficiency	Chalk and talk, PPT	
	24	Class AB output stage, Class C tuned Amplifier	Chalk and talk, PPT	
4	25	Op-amp DC and AC Amplifiers	Chalk and talk, PPT	20
	26	DAC – Weighted resistor and R-2R ladder	Chalk and talk, PPT	
	27	ADC- Successive approximation type	Chalk and talk, PPT	
	28	Small Signal half wave rectifier, Absolute value output circuit	Chalk and talk, PPT	
	29	First order active low-pass and high-pass Butterworth filters	Chalk and talk, PPT	

	30	Second order active low-pass and high-pass Butterworth filters	Chalk and talk, PPT	
	31	Band-pass filters, Band reject filters.	Chalk and talk, PPT	
	32	**555 Timer and its applications:** Monostable and Astable Multivibrators.	Chalk and talk, PPT	
5	33	Power Electronic Systems and Applications	Chalk and talk, PPT	20
	34	Power Electronic Converters AC - DC, & AC - AC	Chalk and talk, PPT	
	35	Power Electronic Converters DC - DC & DC - AC	Chalk and talk, PPT	
	36	Static Anode-Cathode characteristics and Gate characteristics of SCR	Chalk and talk, PPT	
	37	Turn-ON methods, Turn-off Mechanism,	Chalk and talk, PPT	
	38	Turn-OFF Methods: Natural and Forced Commutation – Class A	Chalk and talk, PPT	
	39	Resistance Firing Circuit, Resistance capacitance firing circuit	Chalk and talk, PPT	
	40	Unijunction Transistor: Basic operation and UJT Firing Circuit.	Chalk and talk, PPT	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on BJT Biasing, Small signal operation and Models & MOSFETs	Students study the Topics and will prepare for Final Exam.	Module-1 of the syllabus	3	Individual Activity	Book 1 of the text list.
2	Assignment 2: University Questions on MOSFET Amplifier & Oscillators	Students study the Topics and will prepare for Final Exam.	Module-2 of the syllabus	6	Individual Activity.	Book 1 of the text list.
3	Assignment 3: University Questions on Feedback & Power Amplifiers	Students study the Topics and will prepare for Final Exam.	Module-3 of the syllabus	9	Individual Activity.	Book 1 of the text list.
4	Assignment 4: University Questions on Op-Amp Circuits & 555 Timer	Students study the Topics and will prepare for Final Exam.	Module-4 of the syllabus	12	Individual Activity	Book 3 of the text list.
5	Assignment 5: University Questions on Power Electronic Systems, Thyristors & Gate Trigger Circuit	Students study the Topics and will prepare for Final Exam.	Module-5 of the syllabus	15	Individual Activity	Book 3 of the text list.

14.0 University Result

NEW SCHME

15.0 QUESTION BANK

Module – 1

1. Explain the design constraints of a classical discrete-circuit biasing arrangement with circuit and relevant equations. How does RE provide a negative feedback action to stabilize the bias current?
2. Considering the conceptual circuit of common emitter configuration, derive the expressions for gm, r_Π & re and give relation between r_Π & re.
3. State the disadvantage of fixed V_{GS} biasing technique and explain how stability of operating point is achieved in drain to gate feedback resistor biasing technique in a MOSFET amplifier.
4. Explain hybrid Π model for bipolar junction transistor and give the relation between different currents
5. Write different equations of transconductance and give conclusions from each equation.
6. With the help of small signal operation of MOSFET derive equation for transconductance, gm= $K'_nW/LVov$.
7. A BJT having β=100 is biased at a DC collector current of 1mA. Find the value of gm, re and r_Π at the bias point.

Module -2

1. With the help of circuit diagram explain different basic configurations of MOSFET
2. Explain the common source amplifier without source resistance to find its characteristic parameters Rin, Avo, Ro, Av & Gv.
3. Explain the common source amplifier with source resistance to find its characteristic parameters Rin, Avo, Ro, Av & Gv
4. Explain characteristics parameters of source followers with neat circuit diagram and necessary equations.
5. Explain the internal capacitances of a MOSFET and hence draw the high frequency small signal model of MOSFET.
6. Derive the expression for high frequency response of a common source amplifier; also draw the high frequency curve.
7. Derive the expression for low frequency response of a common source amplifier; also draw the high frequency curve.
8. Draw and explain three frequency band response of a common source amplifier.
9. With neat diagram explain BJT RC phase shift oscillator.
10. With neat diagram explain crystal oscillator.
11. With neat diagram explain Colpitts oscillator.

Module -3

1. Explain any three properties of negative feedback.
2. With neat block diagram and circuit diagram explain voltage amplifier.
3. With neat block diagram and circuit diagram explain current amplifier.
4. With neat block diagram and circuit diagram explain transconductanse amplifier.
5. With neat block diagram and circuit diagram explain transresistance amplifier.
6. Explain with neat block diagram and circuit diagram feedback current amplifier and find equation for current gain, feedback factor, feedback gain and approximate loop gain.
7. With neat block diagram explain how input and output resistance of series shunt feedback amplifier changes with negative feedback consider ideal situation.
8. Explain with neat circuit diagram working of class A output stage, its transfer characteristics and find power conversion efficiency.
9. Explain with neat circuit diagram working of class B output stage, its transfer characteristics and find power conversion efficiency.

10. Explain with neat circuit diagram working of class AB output stage, its transfer characteristics and find its output resistance.
11. Explain with neat circuit diagram working of transformer coupled class A output stage and find power conversion efficiency.

Module – 4

1. Explain with neat circuit diagram noninverting amplifier and derive expressions for close loop gain, input resistance and output resistance.
2. Explain with neat circuit diagram inverting amplifier and derive expressions for close loop gain, input resistance and output resistance.
3. What is R-2R network type DAC? Explain with relevant expressions.
4. Explain the working of a Successive Approximation type of ADC.
5. Explain with a neat circuit diagram, the working of a small signal half wave precision rectifier using an Opamp.
6. Draw and explain the circuit and frequency response of a first order low pass filter.
7. Draw and explain the circuit and frequency response of a second order low pass filter.
8. Draw and explain the circuit and frequency response of a first order high pass filter.
9. Draw and explain the circuit and frequency response of a second order high pass filter.
10. Explain the operation of 555 timer as a astable multivibrator with relevant expressions.
11. Explain the operation of 555 timer as a monostable multivibrator with relevant expressions.

Module – 5

1. What is power electronics? Mention its industrial applications.
2. Explain gate characteristics of thyristors
3. Explain various turn on methods of thyristors
4. Explain various turn off methods of thyristors
5. Explain all four types of power converters and mention the nature of input and output power in each case.
6. Explain the working of the synchronized UJT firing circuit with neat circuit diagram and waveforms.
7. What is commutation? What are the methods of commutation? Explain with necessary circuit diagram and waveforms Class A commutation for series LC with load.
8. Explain the working of the R & R-C firing circuit for thyristor triggering circuits with neat circuit diagram and waveforms.

Prepared by	Checked by		
Prof. D. M. Kumbhar	Prof. S. S. Patil	HOD	Principal

Subject Title	**Analog and Digital Electronics Lab**		
Subject Code	**21EC35**	**CIE Marks**	50
Number of Lecture Hrs/Week /	02 Hours Laboratory	**SEE Marks**	50
RBT Level	L1, L2, L3	**Exam Hours**	03
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. D M Kumbhar	**Designation:** Assistant Professor	**Experience :Teach- 15** years (Ind 07years)
No. of times course taught: 01	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I & II	Analog Electronics Circuits
02	ECE	I & II	Op-Amp
03	ECE	I & II	Digital Electronics

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	I & II	Basic electrical & electronics subjects

2.0 Course Objectives

This laboratory course enables students to

- Understand the electronic circuit schematic and its working
- Realize and test amplifier and oscillator circuits for the given specifications
- Realize the op-amp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
- Study the static characteristics of SCR and test the RC triggering circuit.
- Design and test the combinational and sequential logic circuits for their functionalities.
- Use the suitable ICs based on the specifications and functions.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	Cognitive Level	PO's
CO1	Design and analyze the BJT/FET amplifier and oscillator circuits.	U	1,2,3,4,5,6,7,8,9,10,11,12
CO2	Design and test Op-amp circuits to realize the mathematical computations, DAC and precision rectifiers.	U	1,2,3,4,5,6,7,8,9,10,11,12
CO3	Design and test the combinational logic circuits for the given specifications.	U	1,2,3,4,5,6,7,8,9,10,11,12
CO4	Test the sequential logic circuits for the given functionality.	U	1,2,3,4,5,6,7,8,9,10,11,12
CO5	Demonstrate the basic electronic circuit experiments using SCR and 555 timers.	U	1,2,3,4,5,6,7,8,9,10,11,12
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments:

1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
3	Design and setup the circuits using op-amp: i)Adder, ii)Integrator, iii)Differentiator and iv) Comparator
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.
5	Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor & Full subtractor using NAND gates, (c) 4-variable function using IC74151 (8:1MUX).
6	Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa
7	a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii)T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.
8	Realize a) Design Mod –N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N Counter using IC 7490/7476 c) Synchronous counter using IC 74192
9	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
10	Pseudo random sequence generator using IC 7495
11	Test the precision rectifiers using op-amp: i)Half wave rectifier ii)Full wave rectifier
12	Design Monostable and a stable Multivibrator using 555 Timer.

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	VII/VIII	Project work	Analog & Digital Circuits based concept

6.0 relevance to real world

SL No	Real World Mapping
01	Design analog circuits using OPAMPs for different applications
02	Design digital circuits using digital IC's for different applications
02	Hobby/Mini projects
03	Home appliances/controlling of equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Simulation software like Simulink, PSpice and Proteus.
02	NPTEL	Assembly Application

8.0 Books Used and Recommended to Students

Text Books

1. Fundamentals of Electronic Devices and Circuits Lab Manual, David A Bell, 5th Edition, 2009, Oxford University Press.
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018. ISBN: 978-93-325-4991-3.
3. Fundamentals of Logic Design, Charles H RothJr., Larry L Kinney, Cengage Learning, 7th Edition.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

9) https://nptel.co.in
10) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Assessment Details both (CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20Marks (duration 01 hour**)

7. First test at the end of 5th week of the semester
8. Second test at the end of the 10th week of the semester
9. Third test at the end of the 15th week of the semester Two

assignments each of **10 Marks**

10. First assignment at the end of 4th week of the semester
11. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the Cos and Pos for **20Marks** (**Duration 01 hours**)

12. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50marks**

(To have less stressed CIE, the portion of the syllabus should not be common/repeated for any of the methods of the

CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled time table, with common question papers for the subject (**duration 03 hours)**

4. The question paper will have ten questions. Each question is set for20marks.
5. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
6. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored out of 100 shall be proportionally reduced to 50marks.

12.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1	1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.	7
2	2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator	14
3	3	Design and setup the circuits using op-amp: i)Adder, ii)Integrator, iii)Differentiator and iv) Comparator	21
4	4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC triggering circuit.	29
5	5	Design and implement (d) Half Adder & Full Adder using basic gates and NAND gates, (e) Half subtractor & Full subtractor using NAND gates, (f) 4-variable function using IC74151 (8:1MUX).	36
6	6	Realize (iii) Binary to Gray code conversion & vice-versa (IC74139), (iv) BCD to Excess-3 code conversion and vice versa	43
7	7	c) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii)T Flip-Flop d) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.	50
8	8	Realize d) Design Mod –N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop e) Mod-N Counter using IC 7490/7476 f) Synchronous counter using IC 74192	64
9	9	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (iii)using 4 bit binary input from toggle switches and (iv)by generating digital inputs using mod-16 counter.	72
10	10	Pseudo random sequence generator using IC 7495	86
11	11	Test the precision rectifiers using op-amp: i)Half wave rectifier ii)Full wave rectifier	93
12	12	Design Monostable and a stable Multivibrator using 555 Timer.	100

13.0 VIVA BANK

1. What are the advantages of integrated circuits?
2. What are the popular IC packages available
3. What is an operational amplifier
4. What is the Internal Structure of op-amp and explain each block in brief?
5. What are the characteristics of an ideal op-amp
6. What are the DC, AC Characteristics of OP-Amp?
7. What is input offset voltage?
8. Define input offset current.
9. Define CMRR of an opamp?
10. What is the effect of high frequency on its performance?
11. What is the need for frequency compensation in practical op-amps?
12. What are the frequency compensation methods?
13. Define slew rate.
14. Can we use IC 741 for high frequency applications?
15. Why slew rate is not infinite in Ideal op-amp?
16. What are the applications of op-amps?
17. What do you mean by a precision diode?
18. What are the applications of precision diode?
19. What are the limitations of the basic differentiator circuit?
20. What are the limitations of the basic Integrator circuit?
21. What is a comparator?
22. What are the applications of comparator?
23. Why can't we use comparator to convert sin wave into square wave?
24. What is a multivibrator?
25. What is monostable multivibrator?
26. What is an astable multivibrator?
27. What is a bistable multivibrator?
28. What is the op Amp based Mono stable multivibrator out put signal pulse width?
29. What is the op Amp based Astable multivibrator out put signal time period and frequency?
30. What are the requirements for producing sustained oscillations in feedback circuits? For sustained oscillations,
31. What are the different oscillators?
32. Where PLL is widely used?
33. What are the basic building blocks of PLL?
34. What are the three stages through which PLL operates?
35. Define lock-in range, capture range, and Pull in time of a PLL:
36. What is a voltage controlled oscillator?
37. On what parameters does the free running frequency of VCO depend on?
38. Give the expression for the VCO free running frequency.
39. Mention some typical applications of PLL:
40. List the broad classification of ADCs.
41. List out the direct type ADCs.
42. List out some integrating type converters.
43. What is integrating type converter
44. Explain in brief the principle of operation of successive Approximation ADC.
45. What are the main advantages of integrating type ADCs?
46. Where are the successive approximation type ADC's used?
47. What is the main drawback of a dual slope ADC?
48. State the advantages of dual slope ADC.
49. Define conversion time.
50. Define resolution of a data converter.
51. What is meant by linearity?
52. What is monotonic DAC?
53. What is a sample and hold circuit? Where it is used?

54. Which samples an input signal and holds on to its last sampled value until the input is sampled again. This is mainly used in analog to digital conversion.
55. Explain the various types of digital to analog converters.
56. Sketch the V-I characteristics of an SCR without gate current and with gate current.
57. What is the advantage of SCR over power Transistor?
58. What is the constructional difference in an inverter Thyristor and converter grade Thyristor?
59. List the methods of turning ON of SCR.
60. Define latching current, Holding current, Break over voltage. Show these on the V-I characteristics of SCR.
61. What is the turn-on time of a Thyristor?
62. What is the turn-off time of a Thyristor?
63. Why is SCR called as latching device?
64. Why pulse triggering of SCR is preferred over single or DC triggering?
65. List the important ratings of SCR.
66. What purpose a resistor in series with gate serves?
67. Sketch the characteristics of Triac.
68. What are the terminals of Triac?

13.0 University Result

Examination	Total Students	S+	S	A	B	C	D	E	F	% Passing

Prepared by	Checked by		
Prof. D. M. Kumbhar	Prof. S. S. Patil	HOD	Principal

Subject Title	**Social Connect and Responsibility**		
Subject Code	21UH36/ 21SCR36	**Activity & Reports (10) x 5**	50
Number of Lecture Hrs/Week /	01(P)	**Exam Marks (appearing for)**	50
Total Number of Lecture Hrs	15 Lab Slots	**Exam Hours**	03
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. Sachin S Patil	**Designation:** Assistant Professor	**Experience:**19 years
No. of times course taught: 00	**Specialization:** VLSI Design & ES	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Students should have the knowledge of basic subjects	1 & 2	Universal Human Values

2.0 Course Objectives

- Enable the student to do a deep drive into societal challenges being addressed by NGO(s), social enterprises & The government and build solutions to alleviate these complex social problems through immersion, design & technology.
- Provide a formal platform for students to communicate and connect with their surroundings.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

CO's	Course Outcome	Cognitive Level	PO's
206.1	Develop an eco-friendly relationship for saving the natural resources and preservation of nature.	U	
206.2	Develop multicultural awareness and appreciation for Music and Drama by exposing learners to various forms of Art.	U	
206.3	Understand the concept of agricultural operations.	U	
206.4	Develop an eco-friendly relationship for saving the natural resources and preservation of nature.	U	
206.5	Describe the regional culinary practices and its importance in day-to-day life	U	
Total Hours of instruction		**15**	

4.0 Course Content

Practical/Theory		
Modules	**Teaching Hours**	**Bloom's Taxonomy (RBT) level**
Module 1		
Plantation and adoption of a tree: Plantation of a tree that will be adopted for four years by a group of B.Tech. students. They will also make an excerpt either as a documentary or a photoblog describing the plant′s origin, its usage in daily life, and its appearance in folklore and literature.	03	L1

Module -2		
Heritage walk and crafts corner: Heritage tour, knowing the history and culture of the city, connecting to people around through their history, knowing the city and its craftsman, photoblog and documentary on evolution and practice of various craft forms.	03	L1
Module-3		
Organic farming and waste management: usefulness of organic farming, wet waste management in neighboring villages, and implementation in the campus.	03	L1
Module-4		
Water Conservation: knowing the present practices in the surrounding villages and implementation in the campus, documentary or photo blog presenting the current practices.	03	L1
Module-5		
Food Walk: City's culinary practices, food lore, and indigenous materials of the region used in cooking.	03	L1

5.0 Relevance to future subjects

Sl. No	Semester	Subject	Topics
01	I/II	Universal Human Values	Social Connectivity

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Connecting to Nature and

7.0 Books Used and Recommended to Students

Reference Books
4. Universal Human Values and Professional Ethics, Dr. Ritu Soryan,2022 5. Universal Human Values and Professional Ethics - S.K. Kataria

8.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
11) https://nptel.co.in
12) http://www.uhv.org.in/uhv-1

9.0 Examination Note

Assessment Details both (CIE and SEE):

Continuous Internal Evaluation (CIE)
After completion of, the social connect, the student shall prepare, with daily diary as reference, a comprehensive report in consultation with the mentor/s to indicate what he has observed and learned in the social connect period. The report should be signed by the mentor. The report shall be evaluated on the basis of the following criteria and/or other relevant criteria pertaining to the activity completed.

Marks allotted for the diary are out of 50.

Planning and scheduling the social connect

Information/Data collected during the social connect

Analysis of the information/data and report writing

Considering all above points allotting the marks as mentioned below-

Excellent	80 to 100
Good	60 to 79
Satisfactory	40 to 59
Unsatisfactoryand fail	<39

Semester End Examination (SEE)

This Jamming session will be conducted at the end of the course for 50 marks

Jamming session includes -Platform to connect to others. Share the stories with others. **Share the experience of Social Connect.** Exhibit the talent like playing instruments, singing, one-act play, art painting, and fine art.

Faculty mentor has to design the evaluation system for the Jamming session.

10.0 Course Delivery Plan

Module No.	Session No.	Content of Lecture	Teaching Method	% Portion Covered
1. Plantation and adoption of a tree	1	Plantation in campus	Activity	20
	2	Excerpt either as a documentary or a photoblog describing the plant's origin, its usage in daily life,	Activity	
	3	Its appearance in folklore and literature.	Activity	
2. Heritage walk and crafts corner	4	Visit Heritage place near to college	Activity	20
	5	Knowing the history and culture of the city, connecting to people around through their history, knowing the city	Activity	
	6	Its craftsman, photoblog and documentary on evolution and practice of various craft forms.	Activity	
3. Organic farming and waste management	7	Visiting nearby Village	Activity	20
	8	Usefulness of organic farming, wet waste management in neighboring villages.	Activity	
	9	Implementation in the campus	Activity	
4. Water Conservation	10	Visiting nearby Village	Activity	20
	11	Knowing the present practices in the surrounding villages.	Activity	
	12	Implementation in the campus, documentary or photo blog presenting the current practices.	Activity	
5. Food Walk	13	Visiting food streets. Or food corners	Activity	20
	14	City's culinary practices, food lore	Activity	
	15	indigenous materials of the region used in cooking.	Activity	

11.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity
1	Activity Report 1: Plantation and adoption of a tree	Students carry the activity and will prepare for Final Exam.	Module-1 of the syllabus	3	Group Activity
2	Activity Report 2: Heritage walk and crafts corner	Students carry the activity and will prepare for Final Exam.	Module-2 of the syllabus	6	Group Activity
3	Activity Report 3: Organic farming and waste management	Students carry the activity and will prepare for Final Exam.	Module-3 of the syllabus	9	Group Activity
4	Activity Report 4: Water Conservation	Students carry the activity and will prepare for Final Exam.	Module-4 of the syllabus	12	Group Activity
5	Activity Report 5: Food Walk	Students carry the activity and will prepare for Final Exam.	Module-5 of the syllabus	15	Group Activity

12.0 University Result

Prepared by	Checked by		
Prof.S .S. Patil	Dr. R.R. Magadum	HOD	Principal

Subject Title	**LIC (Linear Integrated Circuits) Lab using Pspice / MultiSIM**		
Subject Code	**21EC383**	**CIE Marks**	**50**
Teaching Hours/Week (L:T:P: S)	**0:0:2:0**	**SEE Marks**	**50**
Total Number of Lecture Hrs	**6**	**Exam Hours**	**03**
CREDITS – 01			

FACULTY DETAILS:		
Name: Prof. Pramod V Patil	**Designation: Asst. Professor**	**Experience: 10 Years**
No. of times course taught: 01	**Specialization: VLSI & Embedded System Design**	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	Basic Electronics
02	Electronics & Communication Engineering	III	Analog Electronics

2.0 Course Objectives

This laboratory course enables students to

- To apply operational amplifiers in linear and nonlinear applications.
- To acquire the basic knowledge of special function ICs.
- To use Multisim/Pspice software for circuit design and simulation

3.0 Course Outcomes

At the end of the course students will be able to:

Sr. No.	Course Outcome	RBT Level	POs
C208.1	Sketch/draw circuit schematics, construct circuits, analyze and troubleshoot circuits containing op-amps, resistors, diodes, capacitors and independent sources.	L3	PO1 to PO12
C208.2	Relate to the manufacturer's data sheets of IC 555 timer and IC µa741 op-amp.	L3	PO1 to PO12
C208.3	Realize and verify the operation of analog integrated circuits like Amplifiers, Precision Rectifiers, Comparators and Waveform generators.	L3	PO1 to PO12
C208.4	Design and implement analog integrated circuits like Oscillators, Active filters, Timer circuits, Data converters and compare the experimental results with theoretical values.	L3	PO1 to PO12
Total Hours of instruction		**06(Weekly)**	

4.0 Course Content

Laboratory Experiments:

1. To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier
2. To realize using op-amps i) Summing Amplifier ii) Difference amplifier
3. To realize using op-amps an Instrumentation Amplifier
4. To realize using op-amps i) Differentiator ii) Integrator
5. To realize using op-amps a Full wave Precision Rectifier
6. To realize using op-amps
   - Inverting and Non-Inverting Zero Crossing Detectors
   - Positive and Negative Voltage level detectors
7. To realize using op-amp an Inverting Schmitt Trigger
8. To realize using op-amp an Astable Multivibrator
9. To design and implement using op-amps
   - Butterworth I & II order Low Pass Filter
   - Butterworth I & II order High Pass Filter
10. To design and implement using op-amp a RC Phase Shift Oscillator
11. To design and implement Mono-stable Multivibrator using 555 timer
12. To design and implement 4 - bit R-2R Digital to Analog Converter

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Communication

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Signal Processors
02	Integrators/ Differentiators

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Topic: Lettering, Line, Methods of dimensioning
02	NPTEL	Linear Integrated circuits

8.0 Books Used and Recommended to Students

Text Books
1) Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education, 2018.

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1) https://vtu.ac.in 2) http://www.bookspar.com/engineering-vtu 3) https://www.youtube.com/watch?v=lpXNCwsnxjM&list=PLuv3GM6-gsE3npYPJJDnEF3pdiHZT6Kj3

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	Website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp

11.0 Examination Note

Assessment Details (both CIE and SEE).

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.
The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14th week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.
SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University .All laboratory experiments are to be included for practical examination. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners. Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours

12.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1	1	To realize using op-amp an Inverting Amplifier and Non-Inverting Amplifier	8
2	2	To realize using op-amps i) Summing Amplifier ii)Difference amplifier	16
3	3	To realize using op-amps an Instrumentation Amplifier	24
4	4	To realize using op-amps i) Differentiator ii)Integrator	32
5	5	To realize using op-amps a Full wave Precision Rectifier	40
6	6	To realize using op-amps • Inverting and Non-Inverting Zero Crossing Detectors • Positive and Negative Voltage level detectors	48
7	7	To realize using op-amp an Inverting Schmitt Trigger	56
1	1	To realize using op-amp an Astable Multivibrator	64
2	2	To design and implement using op-amps • Butterworth I & II order Low Pass Filter • Butterworth I & II order High Pass Filter	72
3	3	To design and implement using op-amp a RC Phase Shift Oscillator	80
4	4	To design and implement Mono-stable Multivibrator using 555 timer	88
5	5	To design and implement 4 - bit R-2R Digital to Analog Converter	100

13.0 University Result

Examination	FCD	FC	SC	% Passing
First Time Introduced				

Prepared by	Checked by		
Prof. Pramod V Patil	Prof. Sachin S Patil	HOD	Principal